RFID SysTech'07

Design Methodology of a Voltage Multiplier for Full Passive Long Range UHF RFID

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Outline

1. Introduction
2. System constraints
3. Voltage Multiplier Design
    A. Improving the efficiency
    B. Performing the input impedance
    C. Output Voltage
    D. Steps to follow
4. Examples
5. Conclusions

1. Introduction

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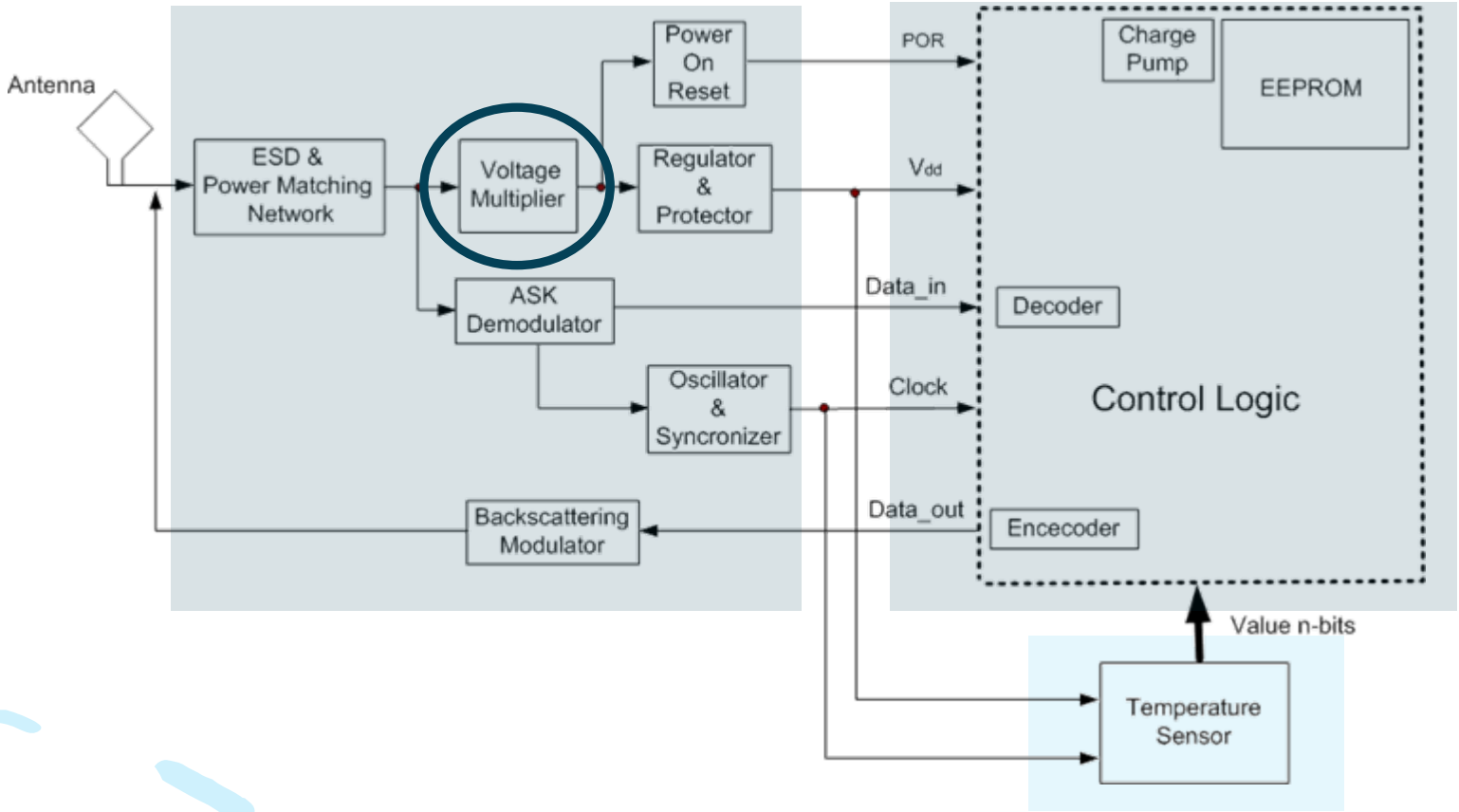
- Blocks Diagram



2. System Constraints

2. System Constraints

- 3 limitations for the communication range:
  - Reader → Tag
    - Minimum input power
    - Minimum input voltage
  - Tag → Reader
    - Probability of error

2. System Constraints

- Minimum input power

Incident power > Tag Power consumption

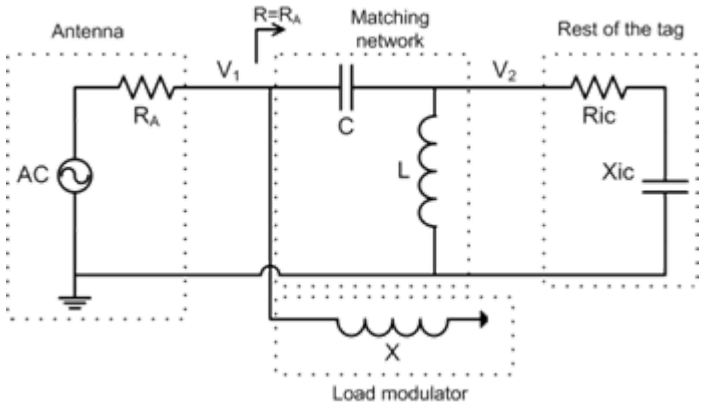
P_{RFin}

$$P_{AV}\frac{4X^2}{R_A^2+4X^2}\geq\frac{1}{\eta}\left(P_{ANA}+P_{DIG}\right) \quad [1] \Rightarrow r_P \leq \sqrt{\frac{P_{eirp}\lambda^2 G X^2 \eta}{4\pi^2\left(R_A^2+4X^2\right)\left(P_{ANA}+P_{DIG}\right)}}$$

[1] G. De Vita and G. Iannaccone, “Design Criteria for the RF section of UHF and Microwave passive RFID transponders” IEEE Trans. Microw. Theroy Tech., vol. 53, no.9, pp. 2985-2989, Sep. 2005

2. System Constraints

- Minimum input voltage
  - Matching Network is required
    - Maximum power transference → increase efficiency
    - Increment of the voltage ($V_2 > V_1$)



$$V_1 = \sqrt{P_{AV} R_A}$$

$$\frac{V_2}{V_1} \cong 0.7 x Q_{mn}$$

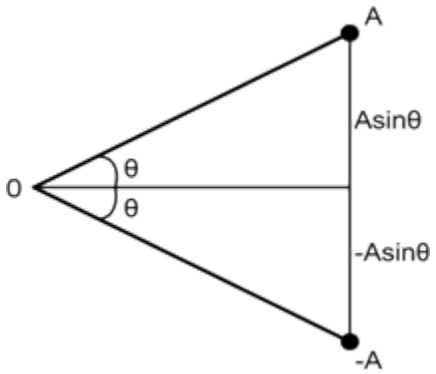
$$\Rightarrow$$

$$r_V \leq \frac{0.7 Q_{mn} \lambda \sqrt{P_{eirp} G R_A}}{4\pi V_{\min}}$$ [2]

[2] D. Pardo, A. Vaz, A. García-Alonso, R. Berenguer. “Design criteria for full passive long range UHF RFID sensor for human body temperature monitoring”. IEEE RFID 2007. Mar. 2007.

2. System Constraints

- Probability of error
  - To achieve appropriate communication → $P_e < 10^{-3}$



BPSK constellation

$$P_e = \frac{1}{2}\left\{ erf\left(\frac{A\sin(\theta)(2\cos(\varphi)-1)}{2\sigma} \right) erf\left(\frac{A\sin(\theta)}{2\sigma} \right) \right\} \leq 10^{-3} \quad [1]$$

[1] G. De Vita and G. Iannaccone, “Design Criteria for the RF section of UHF and Microwave passive RFID transponders” IEEE Trans. Microw. Theroy Tech., vol. 53, no.9, pp. 2985-2989, Sep. 2005

3. Voltage Multiplier Design

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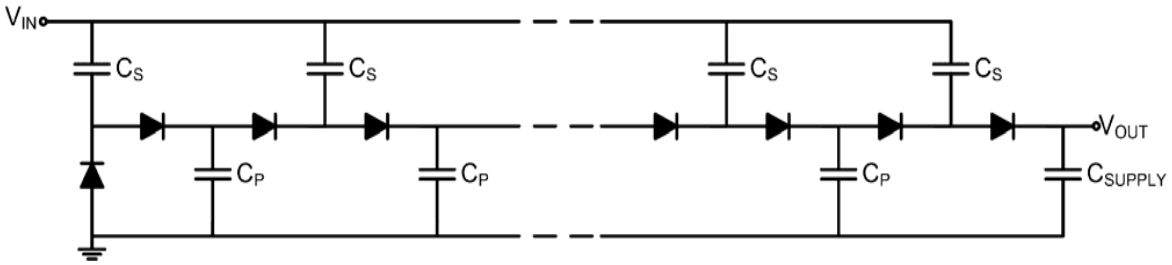
- Dickson's Topology



$$V_{OUT} = K_N N (V_{IN} - V_{fwr})$$

Variable	Guide	
V_{fwr}	↓	Schottky diodes Zero threshold transistors
V_{IN}	↑	Matching network with ↑ Q_{MN}
N	~	Depends on the fixed V_{OUT} (the technology used)
K_N	↑	Depends on diode area, N, C_S and C_P

3. Voltage Multiplier Design

- Detect which one, r_p or r_v, is more restrictive

A. If $r_p < r_v \rightarrow \uparrow$ Efficiency (η)

$$r_P \leq \sqrt{\frac{P_{eirp}\lambda^2 G X^2 \eta}{4\pi^2\left(R_A^2 + 4X^2\right)\left(P_{ANA} + P_{DIG}\right)}}$$

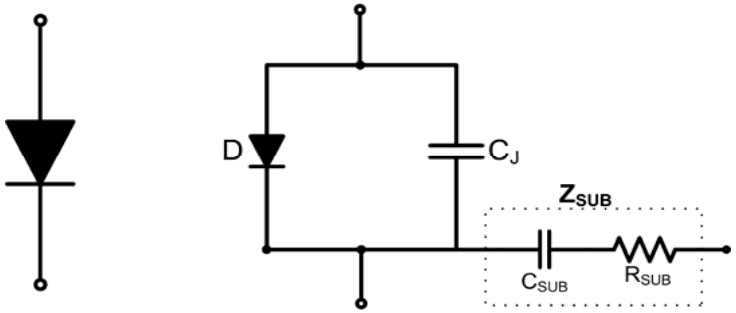
B. If $r_p > r_v \rightarrow \uparrow Q_{mn}$ $\downarrow V_{min}$ $\Rightarrow$ Perform Z_{IN}

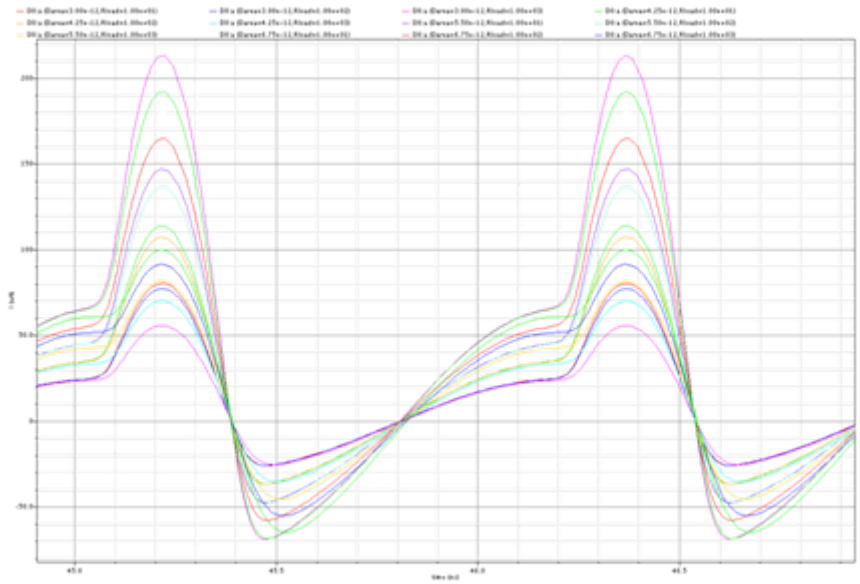
$$r_V = \frac{0.7 Q_{mn} \lambda \sqrt{P_{eirp} G R_A}}{4\pi V_{\min}}$$

3. Voltage Multiplier Design

A. Improving the efficiency ($r_p < r_v$)

1) Optimum Diode Area





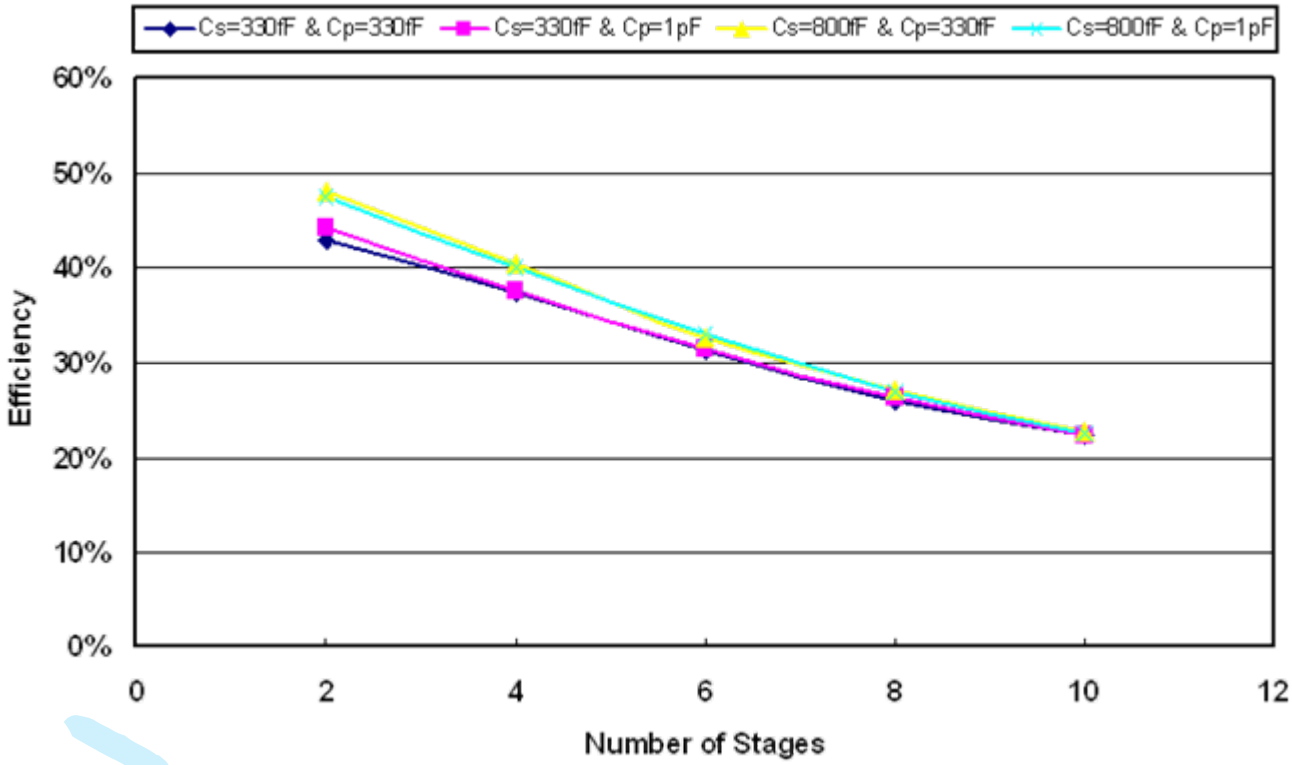
For 868MHz

Optimum Area: 8-10pm²

3. Voltage Multiplier Design

A. Improving the efficiency ($r_p < r_v$)

2) Variation of the number of stages, C_S and C_P values



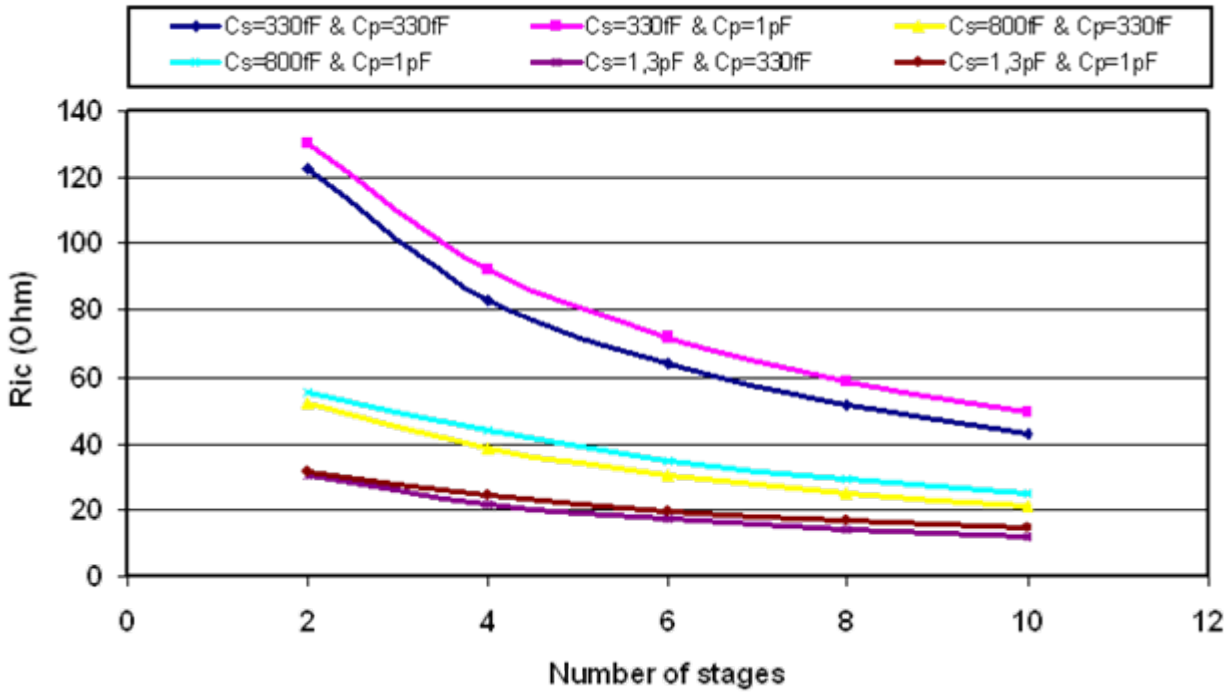
3. Voltage Multiplier Design

B. Performing the input impedance ($r_p > r_v$)

$$V_2 \cong 0.7\sqrt{P_{AV}\left(R_P - R_A\right)}$$

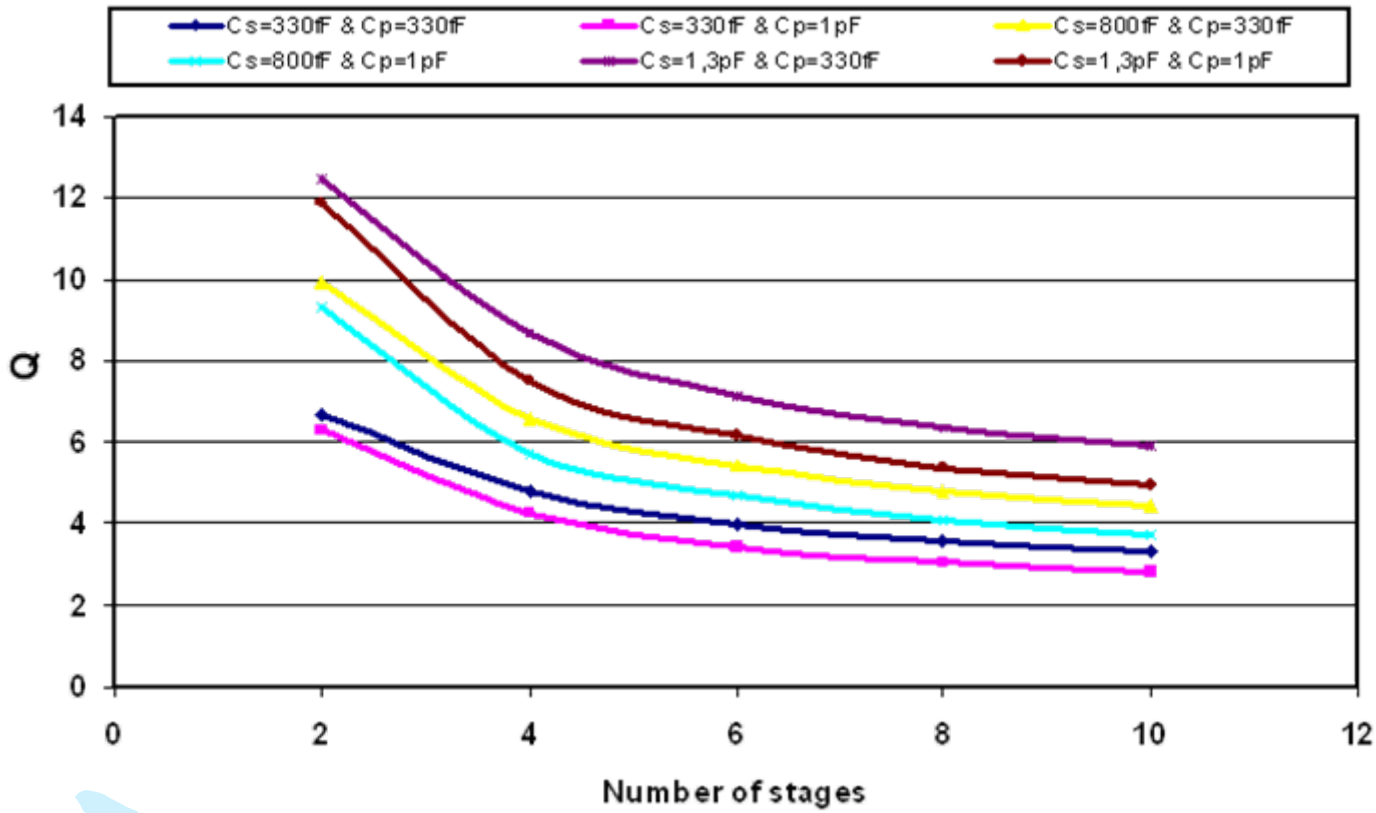
$$R_P = R_{IC}\left(Q^2 + 1\right)$$

$$Q = \frac{X_{IC}}{R_{IC}}$$



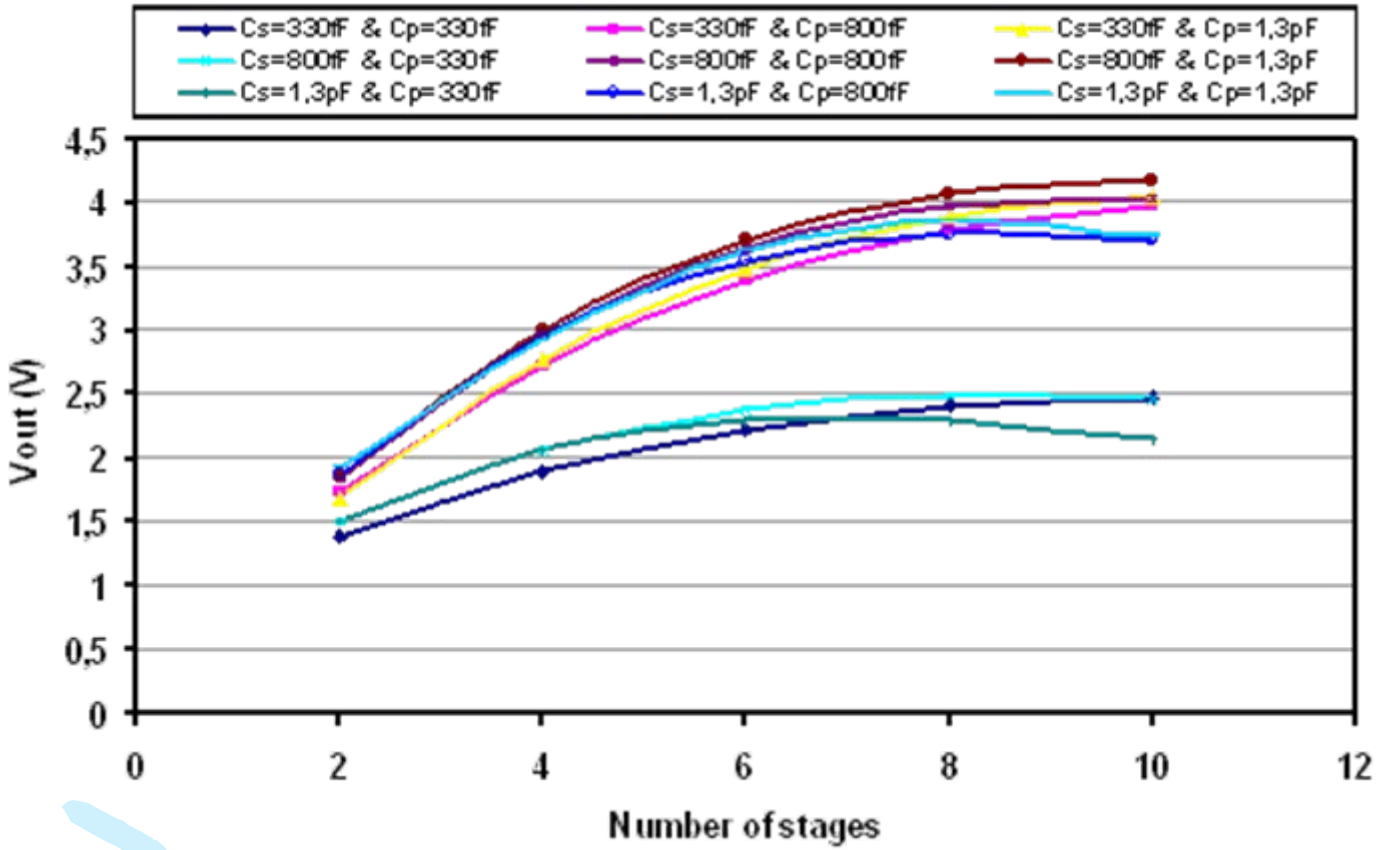
3. Voltage Multiplier Design

B. Performing the input impedance ($r_p > r_v$)



3. Voltage Multiplier Design

C. Output Voltage (V_{OUT})



3. Voltage Multiplier Design

Summary

	η	Q	R_{IC}	V_{OUT}
$\uparrow N$	$\downarrow\downarrow$	$\downarrow$	$\downarrow$	$\uparrow\uparrow$
$\uparrow C_S$	$\uparrow$	$\uparrow\uparrow$	$\downarrow\downarrow$	C_{Sopt}
$\uparrow C_P$	$\sim\uparrow$	$\sim\downarrow$	$\sim\uparrow$	$\sim\uparrow$

$\uparrow V_{OUT}$

C_S and C_P > 400fF
High N
Optimum C_S
High C_P (not decisive)

$\uparrow\eta$

Minimum Number of Stages
High C_S
High C_P (not decisive)

Optimum Z_{IN}

Minimum Number of Stages
High C_S
Low C_P (not decisive)

3. Voltage Multiplier Design

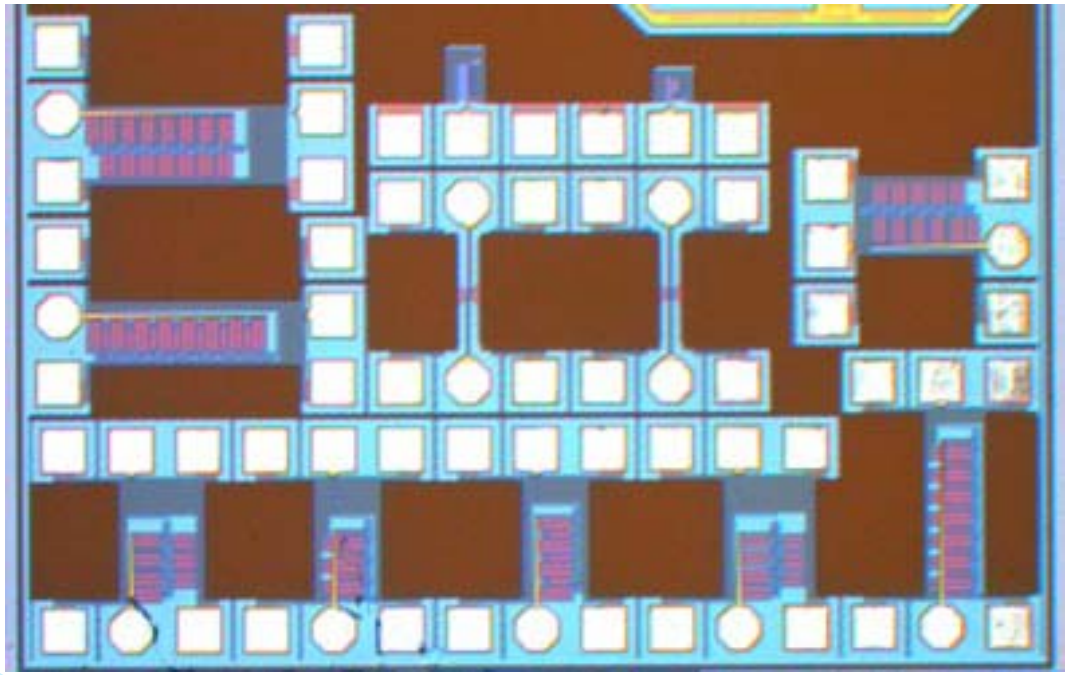
D. Guidelines

1. Determine the optimum diode size
2. Select $V_{OUT} \rightarrow N \rightarrow V_{min}$
3. Detect which one, r_v or r_p, is more restrictive
4. Determine C_S or C_P according to point 3
5. Calculate the input impedance
6. Calculate the matching network

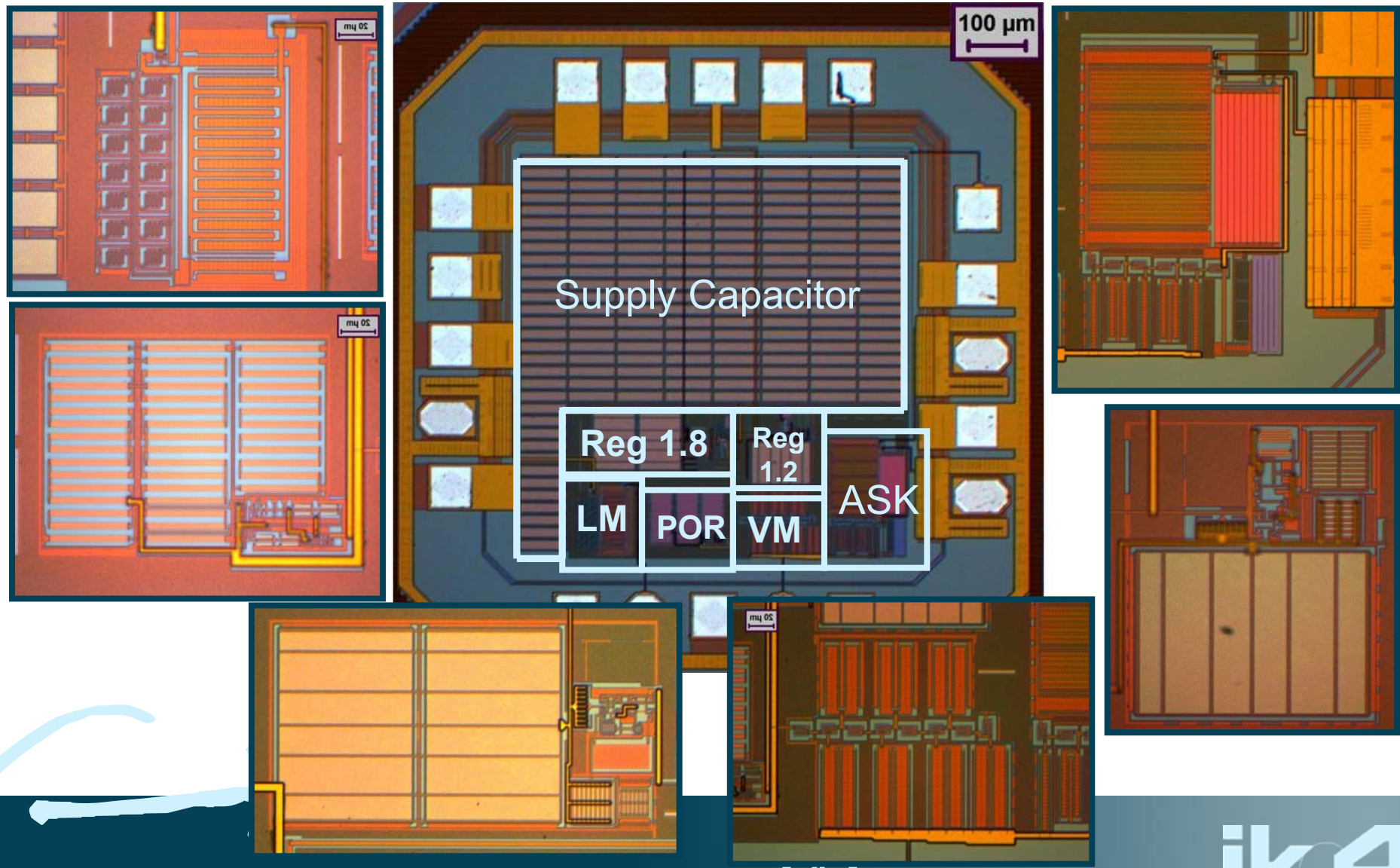
4. Examples

4. Examples

- **Different VM have been fabricated**
  - Number of stages: 4, 6 and 8
  - High Q
  - High Efficiency
  - Optimized for the chip



4. Examples



5. Conclusions

5. Conclusions

- In order to obtain higher reading distances of the tag → VM is critical
- A design for the VM has been presented:
  - Know the real limitation of the RFID system
    - Higher Q
    - Higher Efficiency
    - Trade off between both
  - Design the VM following the guidelines

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