# Optimal Impedance Matching in Passive UHF RFID Sensors

**RFID SysTech 2007**

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# Outline

- Passive UHF RFID Sensors
- Power Recovery System
  - As a DC source
  - As a Load for the Antenna
  - Problems to find Zin
- Method to find the Optimal Zin
- Results
- Conclusions

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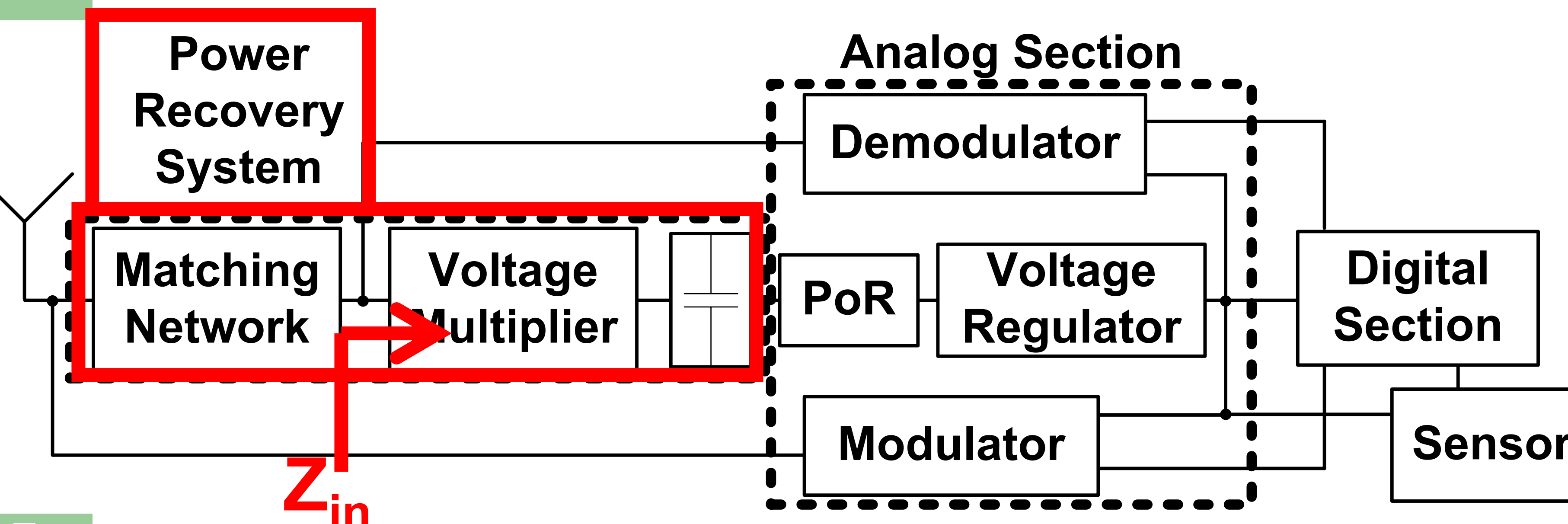
# Passive UHF RFID Sensors

- Passive UHF RFID tags:
  - Battery free
  - Operation range up to 15 meters (Atmel)
  - Data capacity

**Wireless Sensors**

# Passive UHF RFID Sensors

## Passive UHF RFID Tag + Sensor integrated in a single chip



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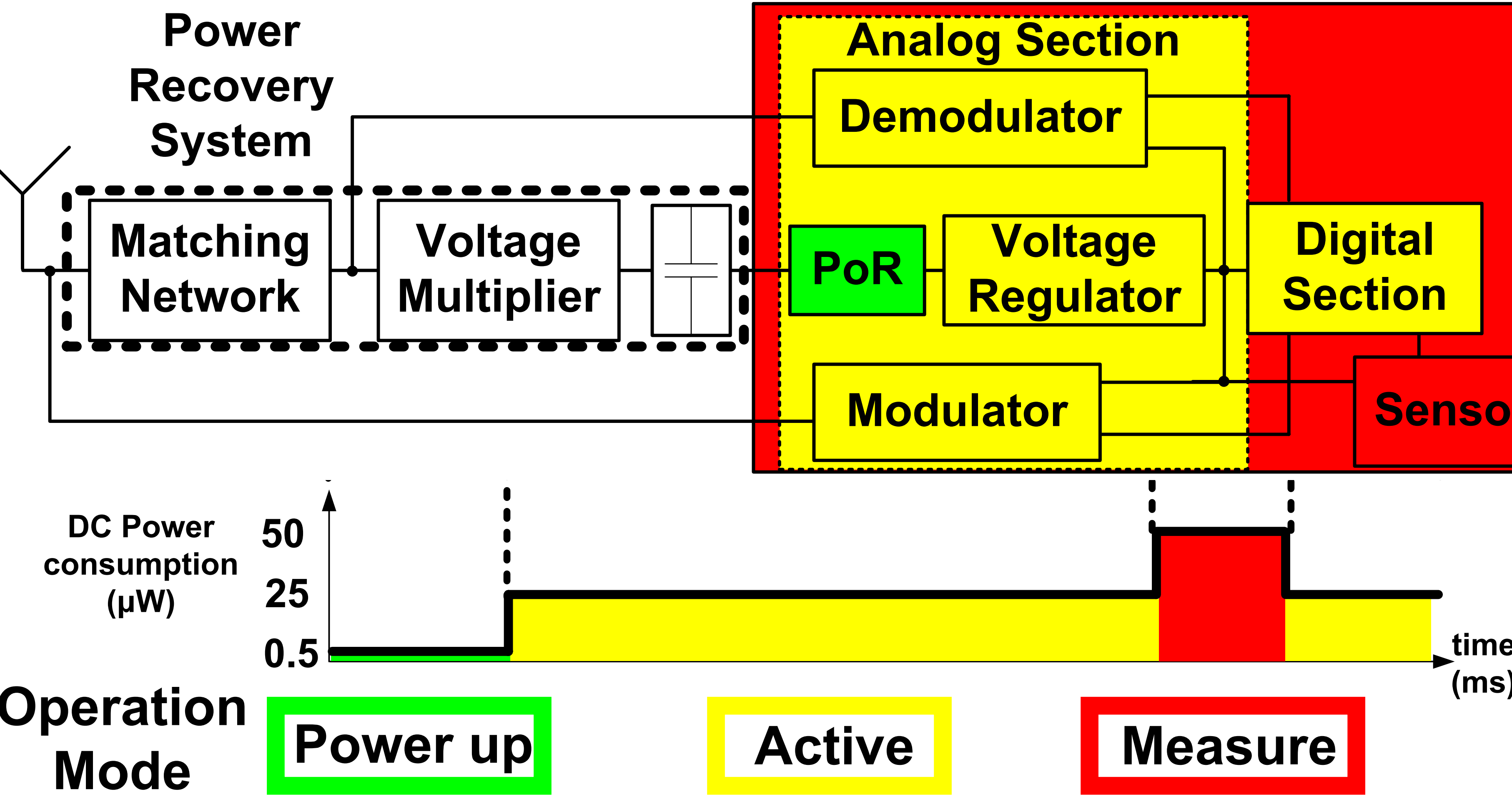
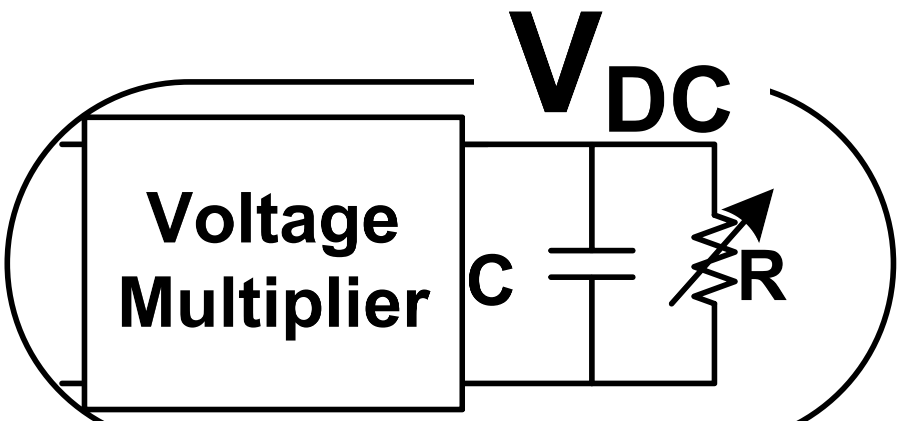
# Power recovery system
## As a DC source

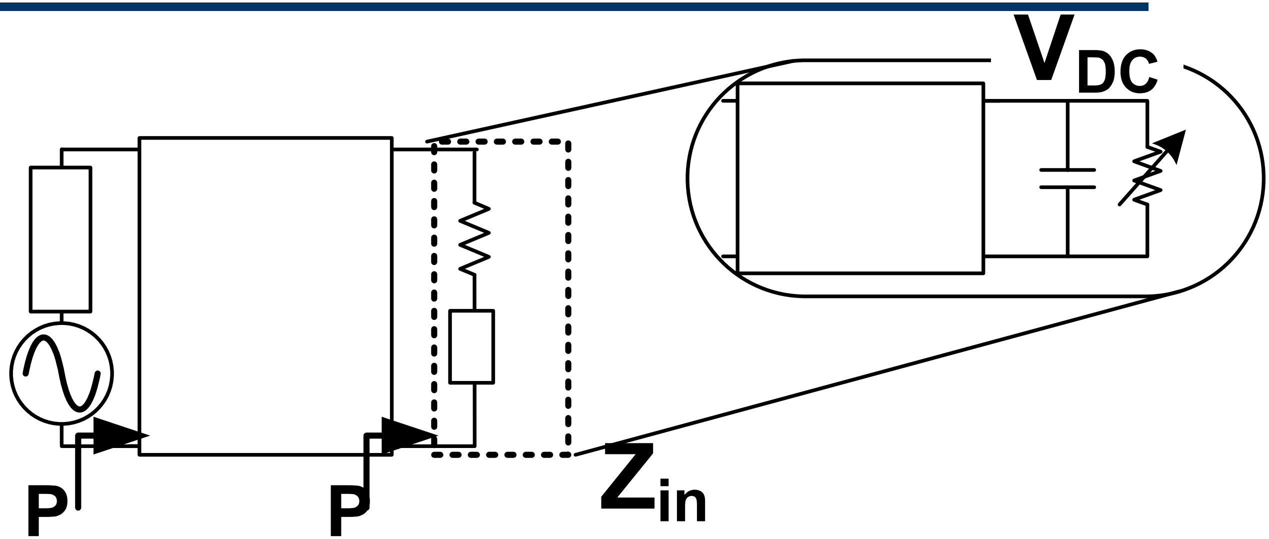


# Power recovery system
## As a DC source

- **Each operation modes can be modeled as a resistance**
- **$V_{DC}$ >= 1.8 V in our technology for all Operation Modes**
- **Power Requirements: Minimum Power required on the Rload for a proper work of the RFID sensor**



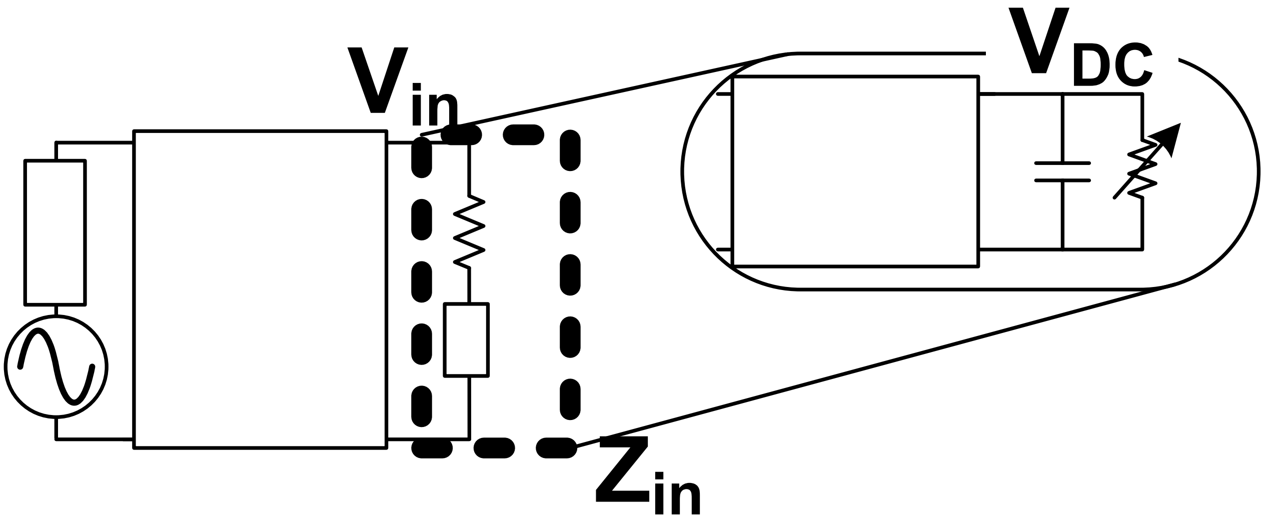
# **Power recovery system**
## As a load for the antenna




- **Maximum Power Transfer → $P_{ant}$=$P_{in}$**
- **Conjugate Matching of $Z_{ant}$ and $Z_{in}$ → Matching Network**

**$Z_{in}$ has to be known**

# Power recovery system
## As a load for the antenna



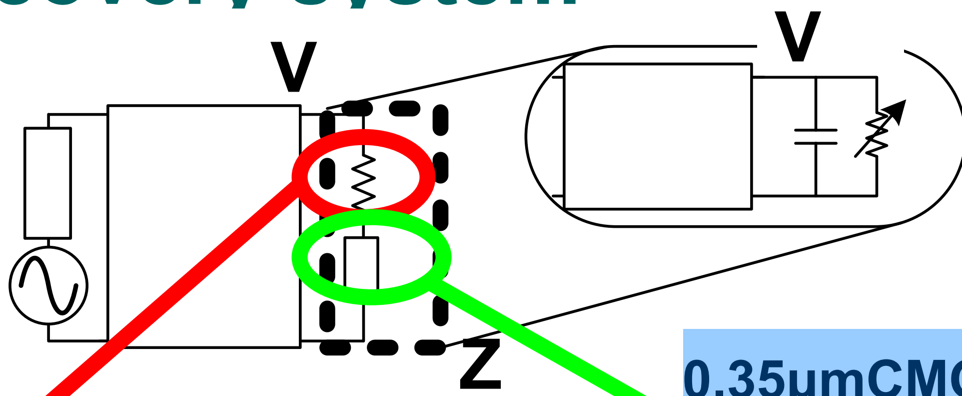

- Vin is the amplitude of the RF signal at the input of the Voltage Multiplier
- Vin is a function of:
  - Pin (Range, Link parameters, Reflections…)
  - Zin

Zant

Matching

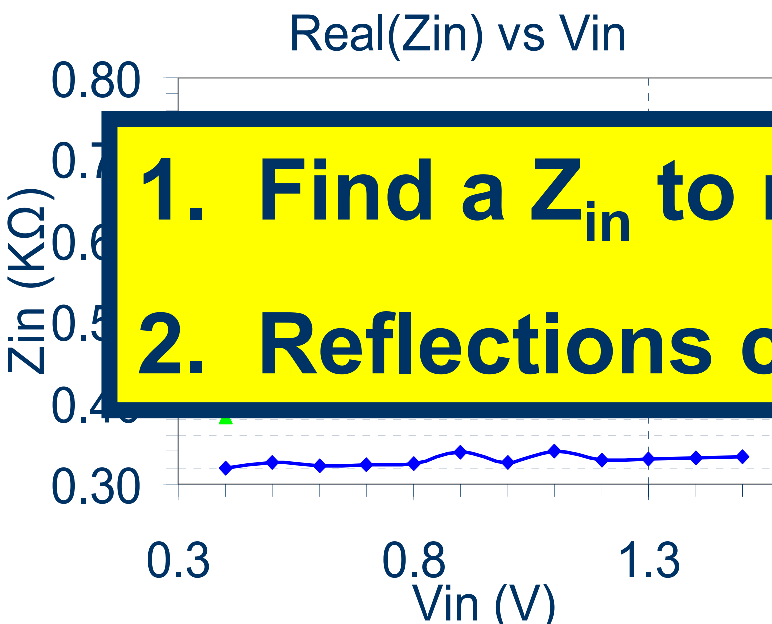
# Power recovery system

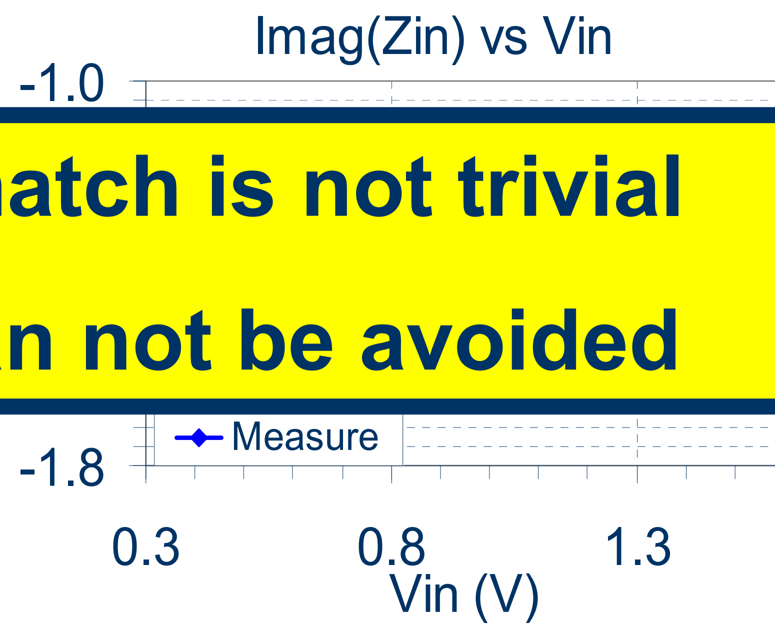
As a




**0.35µmCMOS technology**

**Simulated Input Impedance vs Vin and Operation Mode**

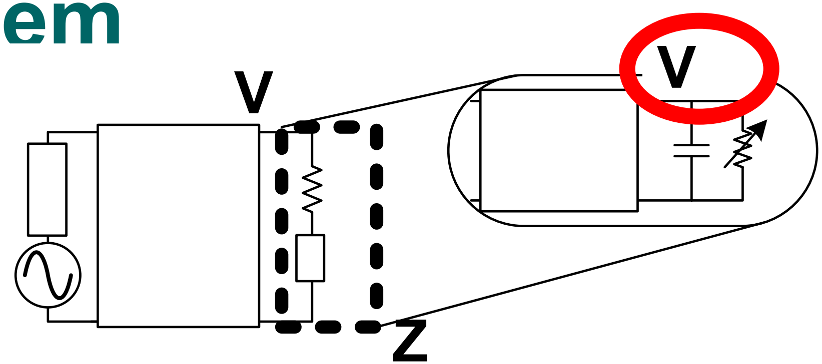


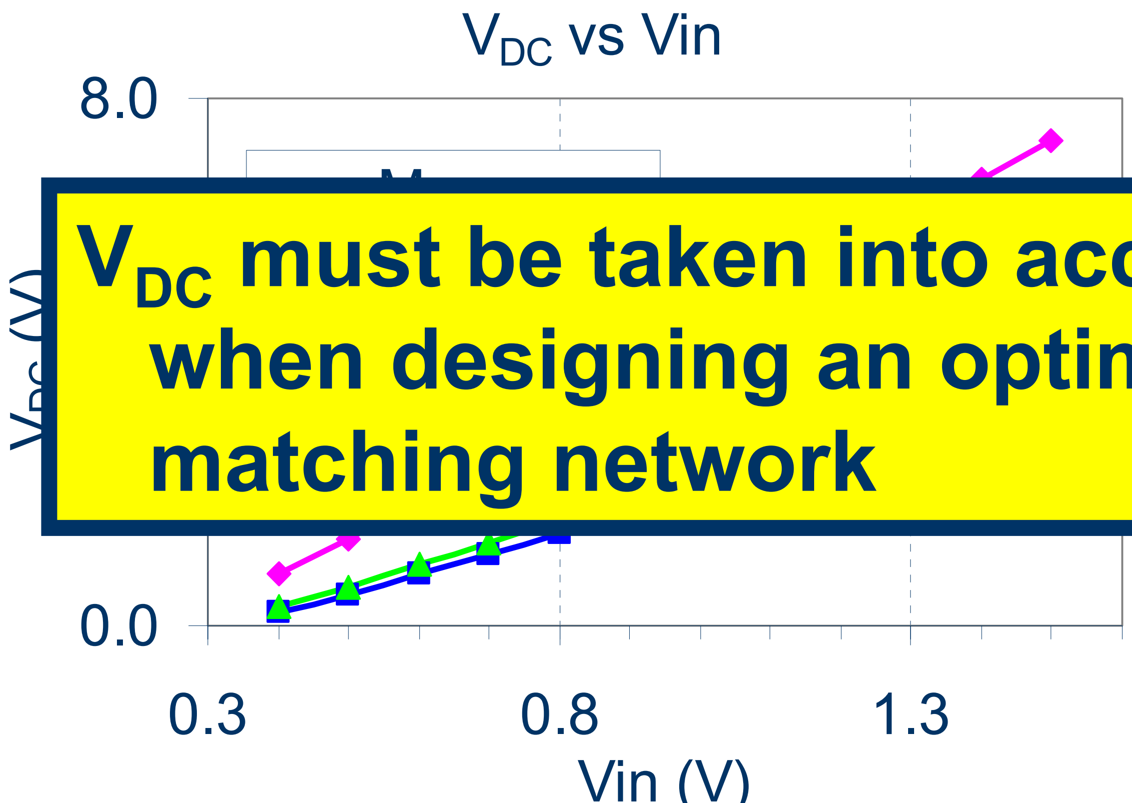




1. **Find a $Z_{in}$ to match is not trivial**
2. **Reflections can not be avoided**

# Power recovery svstem

As a load for the a




The Reflections

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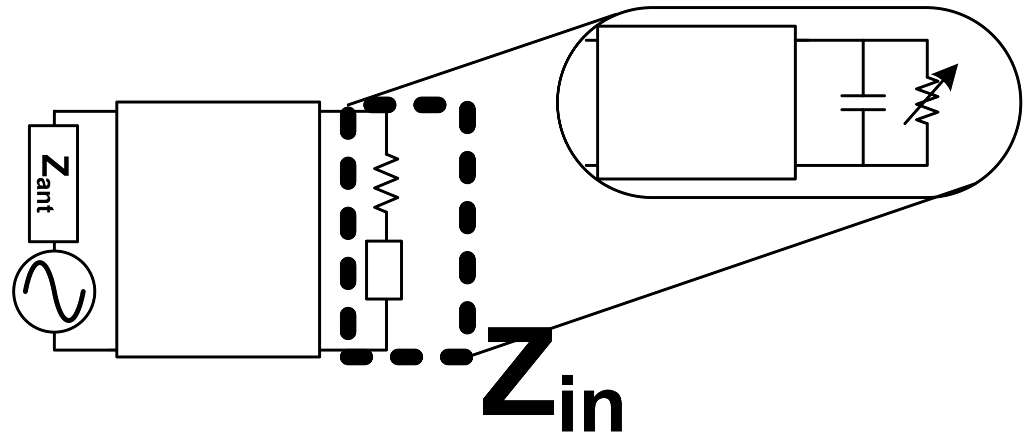
power requirements could be violated.

**$V_{DC}$ must be taken into account when designing an optimal matching network**

# Power recovery system
Problem t(




**To design the Matching Network $Z_{in}$ must be determined**

**PROBLEM**

**$Z_{in}$ is not constant during the link time**

$V_{ant}$sen(wt)

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# Method to find the optimal Zin to match

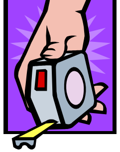
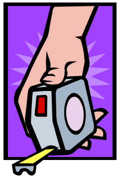
- **What defines $Z_{in}$?**
  - **Design of Voltage Multiplier**
  - **$V_{in} \rightarrow P_{in} \rightarrow$ Range, link parameters (Friis Formula)**
  - **Operation Mode (Tag's Power Consumption)**
- **Which is the optimal $Z_{in}$ to match?**
  - Voltage Multiplier → **Already designed**
  - Link parameters → **pre-defined (freq., gains,…)**
  - The Optimal Zin is the one that for the longest range fulfills all the power requirements

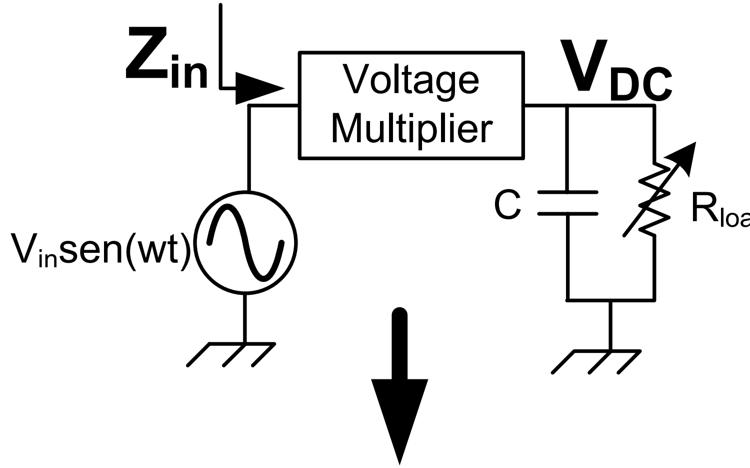
# Method to find the optimal Zin to match

- Analytical solution complex → non-linearity of the VM & dependence on Technology and architecture
- Solution:
  1. Measure-Simulate $\mathbf{Z_{in}}$ and $\mathbf{V_{DC}}$ for every operation mode and for a range of $\mathbf{V_{in}}$
  2. Process the Data with the proposed Algorithm

# **Method to find the opti**
## Impedance Table

- **Voltage Multiplier** → Black Box
- **Range** → each **$V_{in}$** represents a range (Friis Formula)
- **Power Requirements** → Each Operation Mode modeled with a resistance $R_{load}$



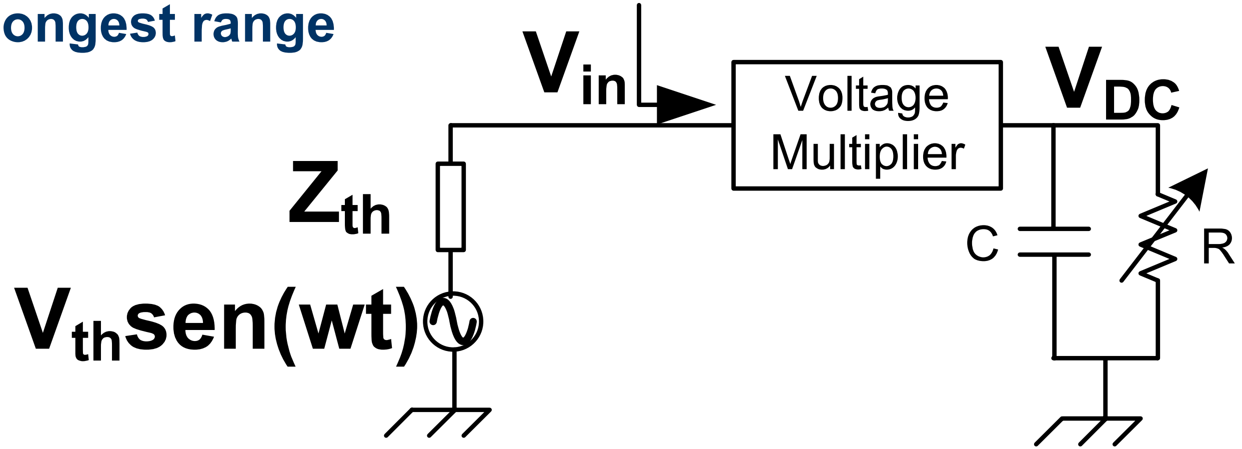

**Impedance Table**

| $V_{in}$ | $R_{load}$ | $V_{DC}$ | $Z_{in}$ |
|---|---|---|---|
| V1 | R1 | $X_1$ | $Z_1$ |
| V1 | R2 | $X_2$ | $Z_2$ |
| V1 | R3 | $X_3$ | $Z_3$ |
| V2 | R1 | $X_4$ | $Z_4$ |
| V2 | R2 | $X_5$ | $Z_5$ |
| | | | |
| Vn | R3 | $X_{3n}$ | $Z_{3n}$ |

# Method to find the optimal Zin to match
Algorithm

**Brute-Force Algorithm**

- **Enumerate all the possible $Z_{th}$ and ranges ($V_{th}$)**
- **Calculate $V_{in}$**
- **Check the Power Requirements in the Impedance Table**
- **Solution: $Z_{th}$ that fulfils the Power Requirements for the longest range**



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# Results

- Voltage Multiplier were designed in 0.35μm CMOS+Schottky process
- Impedance Table from the post-layout simulations

**Voltage Multiplier matched to different Zin**

| Matching | Range (m) | Re($Z_{in}$) (Ω) | Im($Z_{in}$) (Ω) |
|---|---|---|---|
| Measure | 3.75 | 856 | 1150 |
| Active | 3.40 | 320 | 1480 |
| Algorithm | 3.78 | 600 | 1100 |

# Results

**Useful to compare different architectures of VM under the same conditions**

| VM architecture | Range (m) | Re($Z_{in}$) (Ω) | Im($Z_{in}$) (Ω) |
|---|---|---|---|
| **2 stages** | **4.3** | **600** | **1780** |
| **3 stages** | 3.8 | 600 | 1100 |
| **4 stages** | 3.4 | 360 | 800 |
| **6 stages** | 3.8 | 140 | 580 |

# Conclusions

- The design of the Matching Network is not trivial (Influence of the range, power consumption, and voltage multiplier on the $Z_{in}$)
- A method to find the Optimal Input Impedance of a RFID sensor was proposed
- The method was proved in 0.35 CMOS technology
- Useful to compare different VM

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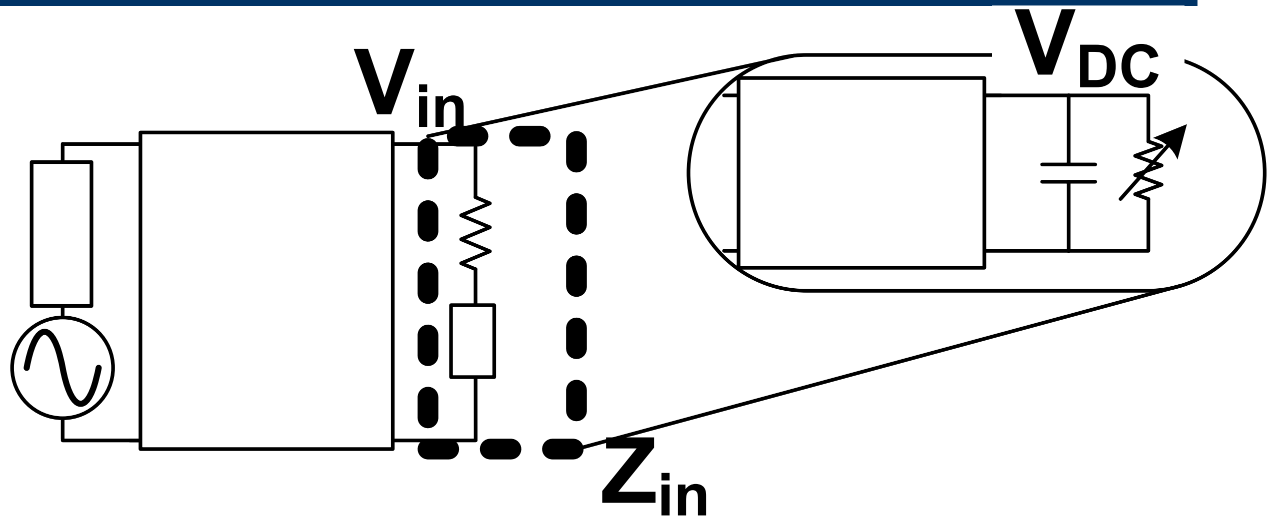


**Friis Formula**

$$P_a = G_r \cdot G_t \cdot P_t \left(\frac{\lambda}{4\pi r}\right)^2$$

**+ Impedance Matching +**

$$P_{diss} = \frac{V_{in}^2}{2R_p}$$

$$V_{in,max} = \sqrt{2 \cdot G_r \cdot G_t \cdot P_t \cdot R_p \cdot \left(\frac{\lambda}{4\pi r}\right)^2}$$